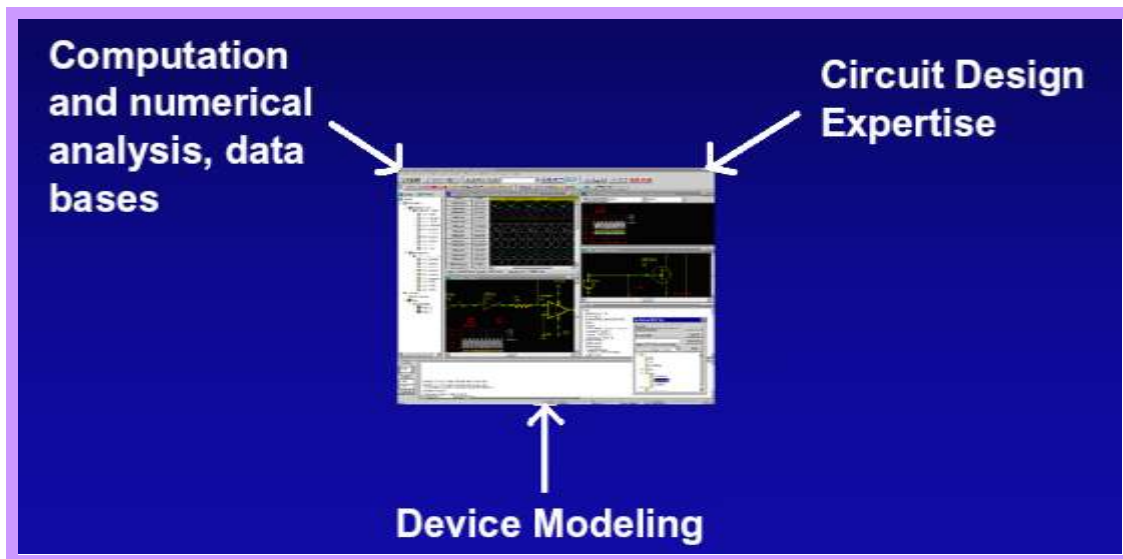


# C-DAC NOIDA

*Organizes  
Workshop  
on*

*“VLSI Chip Design, Verification and Registration Issues”*



*Focus on  
Collaboration across  
diverse domains of knowledge  
and  
Good coupling with industry*

**Date and Time : 20<sup>th</sup> June 2011; 10:00 AM to 5:00 PM**  
**Venue : Auditorium, Academic block, CDAC Noida**

*Address all communications to:*

*Dr. Arti Noor,  
Scientist -E,*

*B-30, Sector-62, CDAC, Noida - 201307.*

*Email: [artinoor@cdacnoida.in](mailto:artinoor@cdacnoida.in); [sunitaprasad@cdacnoida.in](mailto:sunitaprasad@cdacnoida.in);*

*Ph: 0120 3063371-373, 0120-3063380 Fax: 0120 3063374*

## Workshop schedule

*Registration from 09.30 – 10.00 a.m.*

*Inauguration and Welcome Address: 10.00 a.m.*

*Morning Session 10.00 – 1.30 p.m.*

*Layout Registration Process in SICLDR*  
by  
*Ms. Sunita Verma, Additional Director,*  
*SICLDR, DIT, New Delhi.*

*Signal Integrity Issues in VLSI Interconnects*  
by  
*DR B K Kaushik, IIT Roorkee*  
*Coffee Break, 12.00 noon*

*"VLSI Circuit Layout Optimization Methods"*  
by  
*Mr. Sampath Kumar, JSS, Noida*

*Lunch: 1.30 p.m. – 2.00 p.m.*

*Afternoon Session: 2p.m. – 5.00 p.m.*

*"Verification of VLSI System".*  
By  
*Mr. Pratul Kumar, Cadence*

*Coffee Break, 3.00 p.m. - 3.15 p.m.*

*"VLSI Layout Design Using TCAD".*  
By  
*Mr. Amit Kumar, Integrated MicroSystems*

*Closing Remarks: Dr. Arti Noor 5.00 p.m.*

*Interested candidates (Industry People, Faculty and Student) may apply by email to [artinoor@cdacnoida.in](mailto:artinoor@cdacnoida.in) or [sunitaprasad@cdacnoida.in](mailto:sunitaprasad@cdacnoida.in); latest by 17<sup>th</sup> June 2011. Registration is On spot and first come first served basis without any fee(Limited Seats).*