



B-30, Institutional Area, Sector-62,
NOIDA – 201 307
ISO 9001:2008 COMPANY



For information log on to :
<http://www.cdacnoida.in/SoE/pgdevd.asp>
Ph.: 0120 – 3063371-73, 3063361, 9810506024
Fax: 0120 - 3063374
E-mail : info.pgdevd@cdacnoida.in

POST GRADUATE DIPLOMA IN EMBEDDED SYSTEM & VLSI DESIGN

Last date for submitting Application Form:

8th January 2010

Date of Entrance Exam:

16th & 17th January 2010

Date of Result Declaration:

20th January 2009

Last date of Payment of fee for selected candidates:

27th January 2010

Last date of payment of fee for waitlisted candidates:

29th January 2010

Commencement of Course:

1st February 2010

CDAC PROFILE

C-DAC, Noida was established with the mandate to undertake and promote State-of-the-Art Scientific Research & Development of electronics, and to design & develop Electronics Equipment and Systems for the growth of Electronics Industry. The main focus and objective of the organization lies in the development of High skill manpower in various platform of IT industry through HRD activities, transiting the goal of Ministry of Information Technology, Government of India, to bring fruits of Information Technology to every walk of life.

C-DAC, Noida conducts and concentrates on high-end training in Information Technology and other emerging related areas at Post Graduate Levels (Formal & Non-formal), which should provide the basis for sustainable growth and high value added employment to multi-talented I.T. personnel.

PGDEVD - Objectives And Focus Areas

The Post Graduate Diploma in Embedded system and VLSI Design is a six months (24 weeks) full time programme aimed at training engineers from the field of Electronics/Electrical/Computer science / Instrumentation. The programme has two main stream i.e. in areas of Embedded Technology and VLSI Design comprising of 8 main modules. Embedded System Design module will focus on Software Programming, Micro-controller Programming and Embedded Programming in Real Time System, where as VLSI Design Module focus on HDL Programming, FPGA and Synthesis with full custom ASIC Design using EDA tools. This programme will also extend emphasis on various domains e.g. Telecom, e-Security etc. by means of developing application as well as expert sessions from industry.

This unique combination of technologies broadens the scope for the budding engineers. The course is designed with equal emphasis on hardware and software catering to the demands of the industry.

FACILITIES AT CDAC NOIDA :

- A) CDAC, Noida will provide Wi-Fi network wherein
1. Students are required to bring their personal laptops having a wireless LAN Card to the centre for laboratory work (Practicals) throughout the duration of the course. Laptops would be configured by System Administration department for use within the campus. Students should maintain these settings for use within the campus.
 2. In case a student doesn't have a laptop and wants to use lab facility (PC) of organization, student would be required to pay additional fee of Rs. 4000/- per 6 months / semester duration at the time of admission.
- B) Other facilities: State-of-the Art Infrastructure, Well-equipped Library with access to International Journals, Industry focused curriculum and Course Contents leading to International Certification, Creative cum learning work environment, Active placement cell, Experienced and resourceful faculty, Close and constant contact between faculty and students.

ELIGIBILITY CRITERION

- B.E / B.Tech. or equivalent in Electronics/Electrical/Computer/Electronics and Telecommunication/ Instrumentation/ M. Sc (Electronics)
- Students appearing for the final year examination are also eligible.

PLACEMENT CELL

Co-ordinates the task of organizing Campus Interview for the students just before the completion of the course in order to help them to secure attractive jobs. The candidates should keep in mind that selection will depend on the selection criteria and qualitative requirements of the company and the placement cell has no say on the recruitment policy and process of the company visiting the campus. Brief list of companies that visited CDAC, Noida are Wipro, HoneyWell, Satyam, Perot Systems, MBT, IBM, Bharti TeleSoft, Samsung, Network Programs, Quark, NetSys Software, PI Softech etc. Candidates of this programme have got 100% placement opportunities in previous years.

EMBEDDED SYSTEMS DESIGN MODULES		VLSI DESIGN MODULES	
FUNDAMENTALS OF SOFTWARE PROGRAMMING <u>Object Oriented Programming with C++</u> <ul style="list-style-type: none"> • Introduction to C++ programming language • Concepts of OOPS • Classes and objects • Inheritance • Static and dynamic polymorphism • Files and streams 		HDL PROGRAMMING <u>VHDL</u> <ul style="list-style-type: none"> • Basic Language Elements • Behavioral Modeling • Data flow modeling • Structural modeling • Generics & configuration • Subprogram and Overloading • Packages and Libraries • Verification, Writing Test Bench 	
<ul style="list-style-type: none"> • Process Management, Scheduling algorithms • Concurrency of processes and mutual exclusion • Memory Management – Paging & Segmentation • File Management 		<u>VERILOG</u> <ul style="list-style-type: none"> • Intro. to Modeling Styles in Verilog • Compiler Directive, Data Types & Operators • Gate Level, Data Flow & Behavioral Modeling and structure Modeling • Task & Functions • Verification, Writing Test Bench • Switch Level Modeling and UDP • Basics of System Verilog • System Verilog data types, Structure etc. 	
<u>Software Engineering concepts</u> <ul style="list-style-type: none"> • Software Development Life Cycle • Analysis Design & Activities • Testing and Debugging 		<u>FPGA BASED DESIGN</u> <ul style="list-style-type: none"> • Introduction to FPGA architecture • FPGA Design Flow • Logic Synthesis & Implementation • Advanced Design Performance 	
<u>Data structures</u> <ul style="list-style-type: none"> • Introduction to data Structures • Lists ,Stacks & queues • Trees and graphs • Searching & Sorting algorithms 		<ul style="list-style-type: none"> • Design optimization • Back annotating timing & parasitics 	
EMBEDDED PROGRAMMING USING MICROCONTROLLERS <u>8bit Micro-controller programming 32 Bit Micro-controller Programming Using ARM</u>		FPGA & SYNTHESIS <ul style="list-style-type: none"> • Logic Synthesis • Introduction to logic synthesis • Technology mapping • Adding design constraints • Reporting to timing , area, fan-in & fan-out through logic synthesis 	
<ul style="list-style-type: none"> • Introduction to Micro-controllers. • AVR AT90S 8515 Processor Architecture. • Instruction Set. • Interfacing Hardware to the AVR • LED Switches ADC, DAC, Serial Port Interfaces. 		FULL CUSTOM ASIC DESIGN <ul style="list-style-type: none"> • Layout Development, DRC, LVS & Post Layout simulation of basic components of cell library. • Study of Layout design issues like Electro-migration, Antenna effect, Hot electron effect, Latch up, Hot wire effect, drain punch through, • Floor Planning , Placement Planning, and routing 	
<ul style="list-style-type: none"> • Introduction to 32-bit micro controllers • ARM Instruction Set • The ARM GNU Tools and ARM Developer Suite • Overview of ARM and Thumb Instruction Sets • Architectural Support for High-level languages • AMBA • ARM MMU architecture 		SPICE SIMULATION <ul style="list-style-type: none"> • Design Flow • Introduction to SPICE • Circuit descriptions • DC Circuit analysis • Transient analysis • AC circuit analysis • Semiconductor Devices • Schematic Capture, Spectre simulation 	
EMBEDDED PROGRAMMING IN REAL TIME		ADVANCED DIGITAL DESIGN	
<u>Linux systems programming</u> <ul style="list-style-type: none"> • The Linux Kernel in detail • Unix File API • Unix Process API • Inter Process Communication • Multithreading • Network Programming in Linux using sockets. 		<ul style="list-style-type: none"> • Basic overview of digital components • Flip flop operations • Setup and HoldTime Concepts • Design of Mealy and Moore circuits • State machine concepts • State reduction algorithm 	
<u>Real Time OS</u> <ul style="list-style-type: none"> • RTOS Concepts • Introduction to RTLinux/ Monta Vista • IPC in RTLinux / Monta Vista • Programming API of RTLinux/ Debugging 		CMOS VLSI DESIGN CONCEPTS <ul style="list-style-type: none"> • Introduction to MOSFET and its Characteristics • Introduction to CMOS and characteristics • MOS structure and fabrication steps. • CMOS Logic design • Device sizing and analysis 	
<u>D D Programming</u> <ul style="list-style-type: none"> • Kernel configuration (adding modules) • Types of device drivers • Building character drivers • Debugging techniques • Interrupt Handling 			
PROJECT WORK			

SUBMISSION OF APPLICATION & ENTRANCE EXAMINATION

For submission of Application Form, visit our website www.cdacnoida.in. The last date for submission of duly filled application forms is 8th January 2010 at address mentioned below. Same application form is to be used for applying for either or both of the courses i.e PGDEVD & PGDWTA. Examination fee for each of the course is Rs. 300/-. A demand draft of Rs. 300/- or Rs. 600/- (depending on number of courses applied for) in favour of CDAC, Noida payable at NOIDA has to be sent along-with attested photocopies of certificates/marksheets. The last date for sending of DD and attested photocopies of certificates/marksheets is 8th January 2010. There will be an Online Entrance Examination in 4 slots on 16th January and 17th January 2010 at B-30, Institutional area, Sector – 62, NOIDA . The test would be of 2 hrs or 3½ hrs duration consisting of 100 or 170 Multiple Choice Questions depending on number of courses applied for. Test would be based on following depending on course(s) opted.

- Only PGDEVD: Digital Electronics, 'C' Programming Language and General Aptitude
- Both PGDEVD & PGDWTA - Digital Electronics, 'C' Programming Language, General Aptitude, Communication & Computer Networking

REGISTRATION FEES

Fee for the Course is Rs. 45,000/- payable in two installments (First installment Rs. 25,000/- and Second Rs. 20,000/-) by Demand Draft in favour of CDAC, NOIDA payable at Noida. First installment of fee is to be deposited by the selected candidates at the time of admission i.e. on or before 27th January 2010. The second installment is to be paid on the first working day of the programme i.e. 1st February 2010. Course Fee is Non-transferable & Non-refundable. Fee may be refunded with certain conditions only, which will be declared along-with result of the programme. In case, any selected candidate does not pay first installment of fee by 27th January 2010, his seat will be treated as vacant. Such vacant seats will be allotted to candidates in waiting list. Wait listed candidates may contact CDAC, NOIDA at the venue given below on 29th January 2010 for allotment of seats on merit basis.

VENUE: C-DAC, B-30, INSTITUTIONAL AREA, SECTOR – 62, NOIDA, PH. 0120-3063371-73 FAX : 0120-3063374