



B-30, Institutional Area, Sector-62,
NOIDA 201 307
ISO 9001:2008



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POST GRADUATE DIPLOMA IN EMBEDDED SYSTEM & VLSI DESIGN

Last date for submitting Application Form:

3rd July 2009

Date of Entrance Exam:

11th & 12th July 2009

Date of Result Declaration:

16th July 2009

Last date of Payment of fee for selected candidates:

27th July 2009

Last date of payment of fee for waitlisted candidates:

29th July 2009

Commencement of Course:

3rd August 2009

CDAC PROFILE

C-DAC, Noida was established with the mandate to undertake and promote State-of-the-Art Scientific Research & Development of electronics, and to design & develop Electronics Equipment and Systems for the growth of Electronics Industry. The main focus and objective of the organization lies in the development of High skill manpower in various platform of IT industry through HRD activities, transiting the goal of Ministry of Information Technology, Government of India, to bring fruits of Information Technology to every walk of life.

C-DAC, Noida conducts and concentrates on high-end training in Information Technology and other emerging related areas at Post Graduate Levels (Formal & Non-formal), which should provide the basis for sustainable growth and high value added employment to multi-talented I.T. personnel.

PGDEVD Objectives and Focus Areas

The Post Graduate Diploma in Embedded system and VLSI Design is a six months (24 weeks) full time programme aimed at training engineers from the field of Electronics/Electrical/Computer science / Instrumentation. The programme has two main stream i.e. in areas of Embedded Technology and VLSI Design comprising of 8 main modules. Embedded System Design module will focus on Software Programming, Micro-controller Programming and Embedded Programming in Real Time System, where as VLSI Design Module focus on HDL Programming, FPGA and Synthesis with full custom ASIC Design using EDA tools. This programme will also extend emphasis on various domains e.g. Telecom, e-Security etc. by means of developing application as well as expert sessions from industry.

This unique combination of technologies broadens the scope for the budding engineers. The course is designed with equal emphasis on hardware and software catering to the demands of the industry.

FACILITIES AT CDAC NOIDA

- A) CDAC, Noida will provide Wi-Fi network wherein
1. Students are required to bring their personal laptops having a wireless LAN Card to the centre for laboratory work (Practicals) throughout the duration of the course. Laptops would be configured by System Administration department for use within the campus. Students should maintain these settings for use within the campus.
 2. In case a student doesn't have a laptop and wants to use lab facility (PC) of organization, student would be required to pay additional fee of Rs. 4000/- at the time of admission.
- B) Other facilities: State-of-the Art Infrastructure, Well-equipped Library with access to International Journals, Industry focused curriculum and Course Contents leading to International Certification, Creative cum learning work environment, Active placement cell, Experienced and resourceful faculty, Close and constant contact between faculty and students.

ELIGIBILITY CRITERION

B.E/B.Tech. or equivalent in Electronics/Electrical/Computer/Electronics and Telecommunication/ Instrumentation/ M. Sc (Electronics)
Students appearing for the final year examination are also eligible.

PLACEMENT CELL

Co-ordinates the task of organizing Campus Interview for the students just before the completion of the course in order to help them to secure attractive jobs. The candidates should keep in mind that selection will depend on the selection criteria and qualitative requirements of the company and the placement cell has no say on the recruitment policy and process of the company visiting the campus. Brief list of companies that visited CDAC, Noida are Wipro, HoneyWell, Satyam, Perot Systems, MBT, IBM, Bharti TeleSoft, Samsung, Network Programs, Quark, NetSys Software, PI Softech etc. Candidates of this programme have got 100% placement opportunities in previous years.

COURSE CONTENTS

EMBEDDED SYSTEMS DESIGN MODULES		VLSI DESIGN MODULES	
FUNDAMENTALS OF SOFTWARE PROGRAMMING		ADVANCED DIGITAL DESIGN	
<u>Object Oriented Programming with C++</u>	<u>Operating System Concepts</u>	Basic overview of digital components	CMOS VLSI DESIGN CONCEPTS
Introduction to C++ programming language	Process Management, Scheduling algorithms	Flip flop operations	Introduction to MOSFET and its Characteristics
Concepts of OOPS	Concurrency of processes and mutual exclusion	Setup and HoldTime Concepts	Introduction to CMOS and characteristics
Classes and objects	Memory Management – Paging & Segmentation	Design of Mealy and Moore circuits	MOS structure and fabrication steps.
Inheritance	File Management	State machine concepts	CMOS Logic design
Static and dynamic polymorphism	<u>Data structures</u>	State reduction algorithm	Device sizing and analysis
Files and streams	Introduction to data Structures	HDL PROGRAMMING	VERILOG
<u>Software Engineering concepts</u>	Lists, Stacks & queues	<u>VHDL</u>	Intro. to Modeling Styles in Verilog
Software Development Life Cycle	Trees and graphs	Basic Language Elements	Compiler Directive, Data Types
Analysis Design & Activities	Searching & Sorting algorithms	Behavioral Modeling	Gate Level, Data Flow & Behavioral Modeling and structure Modeling
Testing and Debugging		Data flow modeling	Task & Functions
		Structural modeling	Verification, Writing Test Bench
		Generics & configuration	Switch Level Modeling and UDP
		Subprogram and Overloading	Basics of System Verilog
		Packages and Libraries	System Verilog data types.
		Verification, Writing Test Bench	
		FPGA & SYNTHESIS	FPGA BASED DESIGN
		Logic Synthesis	Introduction to FPGA architecture
		Introduction to logic synthesis	FPGA Design Flow
		Technology mapping	Logic Synthesis & Implementation
		Adding design constraints	Advanced Design Performance
		Reporting to timing, area, fan-in & fan-out through logic synthesis	SPICE SIMULATION
		FULL CUSTOM ASIC DESIGN	Design Flow
		Layout Development, DRC, LVS & Post Layout simulation of basic components of cell library.	Introduction to SPICE
		Study of Layout design issues like Electro-migration, Antenna effect, Hot electron effect, Latch up, Hot wire effect, drain punch through, Floor Planning, Placement Planning, and routing	Circuit descriptions
			DC Circuit analysis
			Transient analysis
			AC circuit analysis
			Semiconductor diodes
			Schematic Capture, Spectre simulation
EMBEDDED PROGRAMMING USING MICROCONTROLLERS			
<u>8bit Micro-controller programming</u>	<u>32 Bit Micro-controller Programming Using ARM</u>		
Introduction to Micro-controllers.	Introduction to 32-bit micro controllers		
AVR AT90S 8515 Processor Architecture.	ARM Instruction Set		
Instruction Set.	The ARM GNU Tools and ARM Developer Suite		
Interfacing Hardware to the AVR	Overview of ARM and Thumb Instruction Sets		
LED Switches ADC, DAC, Serial Port Interfaces.	Architectural Support for High-level languages		
	AMBA		
	ARM MMU architecture		
EMBEDDED PROGRAMMING IN REAL TIME			
<u>Linux systems programming</u>	<u>Real Time OS</u>	<u>D D Programming</u>	
The Linux Kernel in detail	RTOS Concepts	Kernel configuration (adding modules)	
Unix File API	Introduction to RTLinux	Types of device drivers	
Unix Process API	IPC in RTLinux	Building character drivers	
Inter Process Communication	Programming API of RTLinux/ Debugging	Debugging techniques	
Multithreading		Interrupt Handling	
Network Programming in Linux using sockets.			
PROJECT WORK			

SUBMISSION OF APPLICATION & ENTRANCE EXAMINATION :

For submission of Application Form, visit website www.cdacnoida.in. The last date for submission of duly filled Application Form is 3rd July 2009. Same application form is to be used for applying for either or both of the courses i.e PGDEVD & PGDWTA. Examination fee for each of the course is Rs. 300/- . A demand draft of Rs. 300/- or Rs. 600/- (depending on number of courses applied for) in favour of CDAC, Noida payable at NOIDA has to be sent along-with attested photocopies of certificates/marksheets. The last date for sending of DD and attested photocopies of certificates/marksheets is 3rd July 2009. There will be an Online Entrance Examination in 4 slots on 11th July 2009 and 12th July 2009 at 2 centres i.e. C-DAC, B-30, Institutional Area, Sector – 62, NOIDA & CIT, MSME-DI Extension Centre, Opp. L Block outer Circle, Connaught Place, New Delhi. The test would be of 2 hrs or 3½ hrs duration consisting of 100 or 170 Multiple Choice Questions depending on number of courses applied for. Test would be based on following depending on course(s) opted.

Only PGDEVD: Digital Electronics 'C' Programming Language General Aptitude

Both PGDEVD & PGDWTA - Digital Electronics 'C' Programming Language, General Aptitude, Communication & Computer Networking

REGISTRATION FEES

Fee for the Course is Rs. 45,000/- payable in two installments (First installment Rs. 25,000/- and Second Rs. 20,000/-) by Demand Draft in favour of CDAC, NOIDA payable at Noida. First installment of fee is to be deposited by the selected candidates at the time of admission i.e. on or before 27th July 2009. The second installment is to be paid on the first working day of the programme i.e. 3rd August 2009. Course Fee is Non-transferable & Non-refundable. Fee may be refunded with certain conditions only, which will be declared along-with result of the programme. In case, any selected candidate does not pay first installment of fee by 27th July 2009, his seat will be treated as vacant. Such vacant seats will be allotted to candidates in waiting list. Wait listed candidates may contact CDAC, NOIDA at the venue given below on 29th July 2009 for allotment of seats on merit basis.

VENUE:

CENTRE FOR DEVELOPMENT OF ADVANCED COMPUTING

B-30, INSTITUTIONAL AREA, SECTOR - 62, NOIDA
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